What is claimed is:

1. A method for forming a top metallization system for high performance integrated circuits, comprising:

providing an integrated circuit comprising a plurality of devices formed in and on a semiconductor substrate, with an overlaying interconnecting metallization structure connected to said devices and comprising a plurality of first metal lines, and having a passivation layer formed thereover, with first openings in said passivation layer to contact pads connected to said first metal lines;

wherein said first openings are as small as 0.1 um; and

forming said top metallization system in said first openings and over said passivation layer, connected to said interconnecting metallization structure, wherein said top metallization system comprises a plurality of top metal lines, in one or more layers, having a thickness substantially greater than said first metal lines, wherein the top metallization system connects portions of said interconnecting metallization structure to other portions of said interconnecting metallization structure.

2. The method of Claim 1 wherein said forming said top metallization system comprises the steps of:

sputtering a thin metal layer, in said first openings and over said passivation layer;

depositing a layer of photoresist over said thin metal layer;

forming second openings in said photoresist over said first openings, said second openings defining metal lines for a first metal layer of said top metallization system;

electroplating a metal layer in said second openings, forming metal lines in said first metal layer;

removing said photoresist; and

removing said thin metal layer in areas not covered by said metal lines.

3. The method of Claim 2 wherein said sputtering a thin metal layer comprises the steps of:

sputtering an adhesion layer; and

sputtering an electroplating seed layer over said adhesion layer.

4. The method of Claim 3 wherein said adhesion layer is selected from the group comprising titanium tungsten (TiW), chromium (Cr), titanium (Ti), and titanium nitride (TiN), and is deposited to a thickness of between about 0.01 and 3 microns.

5. The method of Claim 3 wherein said electroplating seed layer is selected from the group comprising copper (Cu), gold (Au), palladium (Pd) and nickel (Ni) to a thickness of between about 0.05 and 3 microns.

6. The method of Claim 3 wherein said metal layer is selected from the group comprising copper (Cu), gold (Au), palladium (Pd) and nickel (Ni) to a thickness of between about 2 and 100 microns.

7. The method of Claim 1, wherein said top metallization system comprises metal lines formed to a thickness of between about 2 and 1000 times thicker than metal lines in said interconnecting metallization structure, and formed to a width of between about 2 and 1000 times the width of metal lines in said interconnecting metallization structure.

8. The method of Claim 1 wherein said passivation layer is selected from the group comprising PECVD oxide, PECVD nitride, silicon oxynitride, phosphosilicate glass (PSG), borosilicate glass (BSG), borophosphosilicate glass (BPSG), and combinations thereof.

9. The method of Claim 1 further comprising depositing a polymer insulating layer over said passivation layer, and forming second openings in said polymer, insulating layer to expose said contact pads, prior to forming said top metallization system.

10. The method of Claim 9 wherein said polymer is selected from the group comprising polyimide, BCB, paralyne, parylene and elastomer.

11. The method of Claim 10 wherein said second openings in said polymer layer are lined up with said first openings in said passivation layer, and the size of said second openings is greater than that of said first openings.

12. The method of Claim 11 wherein said first openings in said passivation layer are formed to between about 0.1 and 50 um.

13. The method of Claim 2 wherein second and subsequent metal layers of said top metallization system are formed comprising the steps of:

depositing a next polymer layer over underlying metal lines;

forming a via opening to said underlying metal lines through said next polymer layer;

sputtering a next thin metal layer, in said via opening and over said next polymer layer;

depositing a layer of photoresist over said next thin metal layer;

forming next openings in said photoresist over said via openings, said next openings defining metal lines for a next metal layer of said top metallization system;

electroplating a metal layer in said via openings, forming metal lines in said next metal layer;

removing said photoresist; and

removing said next thin metal layer in areas not covered by said next metal lines.

14. The method of Claim 1 wherein polymer layers are formed between said top metal lines, to a thickness of between about 2 and 50 microns, after curing.

15. The method of Claim 7 wherein said polymer layers are thicker than said intermetal dielectric layers formed in said interconnecting metallization structure by a ratio of between about 2 and 500.

16. The method of Claim 1 wherein said forming said top metallization system comprises using a dual damascene technique.

17. The method of Claim 16, wherein said dual damascene technique comprises the steps of:

forming and patterning a polymer layer over said passivation layer, with second openings above said first openings in said passivation layer;

sputtering an adhesion layer in said first and said second openings, and over said polymer layer;

sputtering an electroplating seed layer over said adhesion layer;

electroplating a metal layer in said first and second openings and over said polymer layer;

planarizing said metal layer to form via plugs in said first and second openings;

depositing and patterning a second polymer layer over said via plugs and said polymer layer;

forming a third opening in said second polymer layer to expose at least two of said via plugs;

sputtering a second adhesion layer in said third opening, and over said second polymer layer;

sputtering a second electroplating seed layer over said second adhesion layer;

electroplating a second metal layer in said third opening and over said second polymer layer;

planarizing said second metal layer to form an interconnecting line.

18. The method of Claim 17 wherein said adhesion layers are selected from the group comprising titanium tungsten (TiW), chromium (Cr), titanium (Ti), palladium (Pd), nickel (Ni) and titanium nitride (TiN), and is deposited to a thickness of between about 0.01 and 3 microns.

19. The method of Claim 17 wherein said electroplating seed layers are selected from the group comprising copper (Cu), palladium (Pd), nickel (Ni) and gold (Au), to a thickness of between about 0.05 and 3 microns.

20. The method of Claim 17 wherein said metal layers are selected from the group comprising copper (Cu), palladium (Pd), nickel (Ni) and gold (Au), to a thickness of between about 2 and 100 microns.

21. The method of Claim 1 wherein said forming said top metallization system comprises using a triple damascene technique.

22. The method of Claim 21, wherein said triple damascene technique comprises the steps of:

forming a polymer layer over said passivation layer, with second openings above said first openings in said passivation layer;

depositing a photosensitive polymer layer in said first and second openings, and above said polymer layer;

patterning said photosensitive polymer layer to form a third opening to expose said first and second openings;

sputtering an adhesion layer in said first, second and third openings, and over said photosensitive polymer layer;

sputtering an electroplating seed layer over said adhesion layer;

electroplating a metal layer over said electroplating seed layer;

planarizing said metal layer to simultaneously form via plugs in said first and second openings, and an interconnecting line in said third openings connecting said via plugs together.

23. The method of Claim 1, wherein said top metallization system comprises metal lines formed to a thickness of between about 2 and 1000 times thicker than metal lines in said interconnecting metallization structure, and formed to a width of between about 2 and 1000 times the width of metal lines in said interconnecting metallization structure.

24. The method of Claim 1 wherein said forming each of said top metal lines comprises the steps of:

sputtering a metal layer, in said first openings and over said passivation layer;

forming said top metal lines by patterning and etching said metal layer.

25. The method of Claim 23 wherein said metal layer comprises pure aluminum.

26. The method of Claim 25 wherein said etching comprises the steps of:

depositing and patterning a layer of photoresist over said metal layer; and

dry etching said metal layer using said photoresist as a mask.

27. The method of Claim 25 wherein said etching comprises the steps of:

depositing and patterning a layer of photoresist over said metal layer; and

wet etching said metal layer using said photoresist as a mask.

28. The method of Claim 24 wherein said metal layer is selected from the group comprising copper, nickel, palladium and gold.

29. The method of Claim 28 further comprising the step of sputtering an underlayer in said first openings and over said passivation layer, before said sputtering said metal layer.

30. The method of Claim 29 wherein said underlayer material is selected from a group comprising titanium (Ti), titanium tungsten (TiW), titanium nitride (TiN) and chromium (Cr).

31. The method of Claim 30 wherein said etching comprises the steps of:

depositing and patterning a layer of photoresist over said metal layer; and

dry etching said metal layer and said underlayer using said photoresist as a mask.

32. The method of Claim 30 wherein said etching comprises the steps of:

depositing and patterning a layer of photoresist over said metal layer; and

wet etching said metal layer and said underlayer using said photoresist as a mask.

33. A method for forming a top metallization system for high performance integrated circuits, comprising:

providing an integrated circuit comprising a plurality of devices formed in and on a semiconductor substrate, with an overlaying interconnecting metallization structure connected to said devices and comprising a plurality of first metal lines, and having a passivation layer formed thereover, with first openings in said passivation layer to contact pads connected to said first metal lines;

depositing a polymer insulating layer over said passivation layer, and forming second openings in said polymer, insulating layer to expose said contact pads, wherein said second openings in said polymer layer are lined up with said first openings in said passivation layer, and the size of said second openings is greater than that of said first openings; and

forming said top metallization system in said first openings and over said passivation layer, connected to said interconnecting metallization structure, wherein said top metallization system comprises a plurality of top metal lines, in one or more layers, having a thickness substantially greater than said first metal lines, wherein the top metallization system connects portions of said interconnecting metallization structure to other portions of said interconnecting metallization structure.

34. The method of Claim 33 wherein said first openings in said passivation layer are formed to a size greater than 0.1 um.

35. The method of Claim 33 wherein a first metal layer of said top metallization system is formed using a dual damascene technique to fill vias, and a single damascene technique for interconnecting lines.

36. The method of Claim 33 wherein a first metal layer of said top metallization system is formed using a triple damascene technique.

37. The method of Claim 35 wherein second and subsequent metal layers of said top metallization system are formed using a single damascene technique to fill vias, and a single damascene technique for interconnecting lines.

38. The method of Claim 35 wherein second and subsequent metal layers of said top metallization system are formed using a dual damascene technique.

39. The method of Claim 36 wherein second and subsequent metal layers of said top metallization system are formed using a single damascene technique to fill vias, and a single damascene technique for interconnecting lines.

40. The method of Claim 36 wherein second and subsequent metal layers of said top metallization system are formed using a dual damascene technique.

41. A method for forming a top metallization system for high performance integrated circuits, comprising:

providing an integrated circuit comprising a plurality of devices formed in and on a semiconductor substrate, with an overlaying interconnecting metallization structure connected to said devices and comprising a plurality of first metal lines, and having a passivation layer formed thereover, with first openings in said passivation layer to contact pads connected to said first metal lines;

wherein said first openings are as small as 0.1 um; and

forming said top metallization system in said first openings and over said passivation layer, connected to said interconnecting metallization structure, wherein said top metallization system comprises a plurality of top metal lines, in one or more layers, having a width substantially greater than said first metal lines, wherein the top metallization system connects portions of said interconnecting metallization structure to other portions of said interconnecting metallization structure.

42. The method of Claim 41 wherein a first metal layer of said top metallization system is formed using a dual damascene technique to fill said first openings and for forming interconnecting lines.

43. The method of Claim 42 wherein second and subsequent metal layers of said top metallization system are formed using a single damascene technique to fill vias, and a single damascene technique for interconnecting lines.

44. The method of Claim 42 wherein second and subsequent metal layers of said top metallization system are formed using a dual damascene technique.

45. A semiconductor device structure, comprising:

semiconductor devices formed on a semiconductor substrate, with an overlaying interconnecting metallization structure connected to said devices and comprising a plurality of first metal lines, and having a passivation layer formed thereover, with first openings in said passivation layer to contact pads connected to said first metal lines, wherein said first openings are as small as 0.1 um; and

a top metallization system formed in said openings and over said passivation layer, connected to said interconnecting metallization structure, wherein said top metallization system comprises a plurality of top metal lines, in one or more layers, having a thickness substantially greater than said first metal lines.

46. The structure of Claim 45 wherein a first metal layer of said top metallization system comprises:

a thin adhesion layer, in said first openings and over said passivation layer;

a thin seed layer, formed over said thin adhesion layer; and

a thick metal layer formed over said seed layer.

47. The structure of Claim 46, further comprising a cap layer formed over said thick metal layer.

48. The structure of Claim 47, wherein said cap layer comprises nickel (Ni).

49. The structure of Claim 48 wherein said thin adhesion layer is selected from the group comprising titanium tungsten (TiW), chromium (Cr), titanium (Ti), palladium (Pd), nickel (Ni) and titanium nitride (TiN), and has a thickness of between about 0.01 and 3 microns.

50. The structure of Claim 48 wherein said thin seed layer is selected from the group comprising copper (Cu), palladium (Pd), nickel (Ni) and gold (Au), and has a thickness of between about 0.05 and 3 microns.

51. The structure of Claim 48 wherein said thick metal layer is selected from the group comprising copper (Cu), palladium (Pd), nickel (Ni) and gold (Au), and has a thickness of between about 2 and 100 microns.

52. The structure of Claim 48 further comprising additional metal layers, each of said additional metal layers comprising a thick metal layer formed over a thin seed layer and a thin adhesion layer.

53. The structure of Claim 52 wherein said thick metal layer is selected from the group comprising copper (Cu), palladium (Pd), nickel (Ni) and gold (Au), and has a thickness of between about 2 and 100 microns.

54. The structure of Claim 45 wherein said top metal lines are formed of pure aluminum.

55. The structure of Claim 45 wherein said top metal lines are formed of a material selected from the group comprising copper (Cu), gold (Au), palladium (Pd) and nickel (Ni).

56. The structure of Claim 45, wherein said top metallization system comprises metal lines formed to a thickness of between about 2 and 1000 times thicker than metal lines in said interconnecting metallization structure, and formed to a width of between about 2 and 1000 times the width of metal lines in said interconnecting metallization structure.

57. The structure of Claim 45 further comprising a polymer insulating layer formed over said passivation layer, wherein second openings in said polymer insulating layer are formed over and which are larger than said first openings.

58. The structure of Claim 57 wherein said polymer insulating layer is formed of a material selected from the group comprising polyimide, BCB, paralyne, parylene and elastomer.

59. The structure of Claim 45 further comprising intermetal polymer layers, formed between said top metal lines, to a thickness of between about 2 and 30 microns.

60. The structure of Claim 59 wherein said intermetal polymer layers are thicker than intermetal dielectric layers formed in said interconnecting metallization structure by a ratio of between about 2 and 500.

61. The structure of Claim 57 wherein said intermetal polymer layers are formed of a material selected from the group comprising polyimide, BCB, paralyne, parylene and elastomer.

62. A semiconductor device structure, comprising:

semiconductor devices formed on a semiconductor substrate, with an overlaying interconnecting metallization structure connected to said devices and comprising a plurality of first metal lines, and having a passivation layer formed thereover, with first openings in said passivation layer to contact pads connected to said first metal lines, wherein said first openings are as small as 0.1 um; and

a top metallization system formed in said openings and over said passivation layer, connected to said interconnecting metallization structure, wherein said top metallization system comprises a plurality of top metal lines, in one or more layers, having a thickness substantially greater than said first metal lines;

wherein said top metal lines comprise gold (Au) over a titanium tungsten (TiW) underlayer.

63. A semiconductor device structure, comprising:

semiconductor devices formed on a semiconductor substrate, with an overlaying interconnecting metallization structure connected to said devices and comprising a plurality of first metal lines, and having a passivation layer formed thereover, with first openings in said passivation layer to contact pads connected to said first metal lines, wherein said first openings are as small as 0.1 um; and

a top metallization system formed in said openings and over said passivation layer, connected to said interconnecting metallization structure, wherein said top metallization system comprises a plurality of top metal lines, in one or more layers, having a thickness substantially greater than said first metal lines;

wherein said top metal lines comprise plated copper (Cu) over a copper seed layer formed over a chromium (Cr) underlayer, and wherein said plated copper is covered with a nickel (Ni) cap layer.